

REMARKS

This amendment is in response to the Office Action mailed April 22, 2005. Claims 1 – 11 were pending, and Claims 7 – 11 were allowed, Claims 2 – 6 were objected to, and Claim 1 was rejected.

In response, the Applicant has cancelled Claim 1, amended Claim 2 as an independent claim, and has added new claims 12 – 16.

In the cited Brehmer reference, while an A/D converter is co-located in a pixel block, the A/D converter is a relatively low-speed converter. To one of ordinary skill in the art, Brehmer is teaching a conventional column buffer design including a low-speed converter, which is in agreement with the conventional wisdom that one should avoid high-speed A/D converters, due to the attendant reactance problems and power generation problems. Thus, it appears that the circuit of Brehmer uses column-wise digitization at relatively low pixel rates (100 kHz to 5 MHz) and relatively coarse resolution (8 to 10 bits).


In contrast, the A/D converter of the present invention operates at relatively high speed (> 10 MHz) and with greater than or equal to 12 bit resolution. Thus, it is believed that the newly added claims 12 – 16 are allowable over the cited prior art for at least these reasons.

It is now believed that the present case is now in condition for allowance. If the Examiner believes that a telephone conference will expedite the processing of this application, please contact the undersigned attorney at the listed telephone number.

Respectfully submitted,

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